

ABSTRACT

A virtual to physical address translator in which a requesting process supplements a virtual memory address with a shortcut to a physical address associated with one level of a multi-level virtual address translation table. A second process, such as an I/O process, receives the shortcut and the virtual address and uses an address translator to determine the physical address. In some implementations, the shortcut may be made opaque to the requesting process such that the requesting process cannot determine the physical address represented in the shortcut.

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